In the Specification

Please replace paragraph [0032] of the Specification with the following new paragraph:

[0032] Referring now to Figure 4, a flowchart 400 of the operation of a predictor is shown, according to one embodiment of the present disclosure. The process begins when a new instruction pointer is received in block 402. Then this instruction pointer may be used to create an index into the confidence value pattern history table in block 404 and an index into the predicted value pattern history table in block 408. These indexes may then be used in block 406 to retrieve the confidence count from confidence value pattern history table and in block 410 to retrieve the predicted value from predicted value pattern history table.

Please replace paragraph [0034] with the following new paragraph:

[0034] Referring now to Figure 4B, a flowchart 450 of the repair of speculative global history registers by the architectural global history registers is shown, according to one embodiment of the present disclosure. In block 452, the process may monitor the speculative global history registers and determine which predicates were previously predicted. In block 454, the process executes one of the corresponding instructions that calculates the predicate value. Then in decision block 456, it may be determined whether the prediction was indeed correct when compared with the actually-determined value of the predicate. If so, then the process exits along the YES path and in block 462 the indexed confidence count may be incremented. Then in block 464 the values in the speculative global history registers may be committed to the architectural global history registers. However, if in decision block 456 it is determined that the prediction was incorrect, then the process exits along the NO path and in block 458 the indexed confidence count may be cleared and the predicted value bit may be updated. Then in block 460 the speculative global history registers may be repaired.

Please replace paragraph [0038] with the following new paragraph:

[0038] The Figure 5B system may also include several processors, of which only two, processors 70, 80 are shown for clarity. Processors 70, 80 may each include a local memory controller hub (MCH) 72, 82 to connect with memory 2, 4. As shown in Figure 5B, processor 70 includes processor core 70, and processor 80 includes processor core 84. Processors 70, 80 may exchange data via a point-to-point interface 50 using point-to-point interface circuits 78, 88. Processors 70, 80 may each exchange data with a chipset 90 via individual point-to-point interfaces 52, 54 using point to point interface circuits 76, 94, 86, 98. Chipset 90 may also exchange data with a high-performance graphics circuit 38 via a high-performance graphics interface 92.